

## Optimum Placement of Decoupling Capacitors on Packages and Printed Circuit Boards Under the Guidance of Electromagnetic Field Simulation

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**Abstract** — This paper presents an efficient signal integrity analysis technique for simulating voltage fluctuations on power/ground planes in complex packaging structures. With its unique circuit and electromagnetic field solvers, the value, the number and the location of the decoupling capacitor placed on packages or printed circuit boards can be quickly and effectively evaluated. Examples are provided to demonstrate that how a good decoupling scheme is achieved under the guidance of electromagnetic field simulation.

### INTRODUCTION

**T**HE trend of electronic packaging is toward faster transition speed and more I/O count due to the advances in fabrication technology. As a consequence, many signal integrity problems become increasingly challenging to design engineers. Delta-I noise, also called simultaneous switching noise or power/ground bounce, is one of the problems that become worse with faster device switching speed, more I/Os, and higher clock frequency. The cause of the voltage fluctuations on power/ground reference planes is the transient currents drawn by a large number of drivers switching simultaneously. This noise could degrade the buffer output waveforms, falsely set the latches, and influence the quiet chips due to the coupling between the power distribution and the signal distribution systems.

To ensure the system reliability, the common practice for suppressing voltage fluctuations on power/ground planes is to add decoupling capacitors, which provide the ac ground for the noise and maintain the dc supply voltage. But due to the lack of efficient tools that can evaluate the effects of decoupling capacitors, the number and the value of the decoupling capacitors placed on a package can be either insufficient or excessive. In order to evaluate decoupling capacitors for any real designs, the power/ground plane structures need to be accurately modeled and the Delta-I noise need to be efficiently simulated.

Previously used simple lumped circuit model for power/ground planes such as effective-inductor is not suitable for high-speed packaging structures because as the switching currents flow through vias, they generate electromagnetic waves propagating between metal planes [1]. The voltage fluctuations on the metal planes, therefore, are different at various locations. The simple lumped circuit representation of the power/ground planes can not reflect the electromagnetic wave effects.

Network parameter (such as S, Z, or Y matrices) or R-L-C network representations of power/ground plane structures can be extracted through intensive electromagnetic computations. To fully take into account package resonance and

electromagnetic interactions in packages of a large number of vias, the number of network parameter elements can become formidably large, resulting in long computation times for circuit simulations.

The traditional 3D EM field solvers, such as those based on the finite-difference time-domain methods, can accurately simulate power/ground plane structures, and therefore, provide a way to evaluate decoupling capacitors. But they are not suitable for fast simulation of practical designs with hundreds or thousands of vias/traces and multiple power/ground planes because of their enormous computer resource requirement.

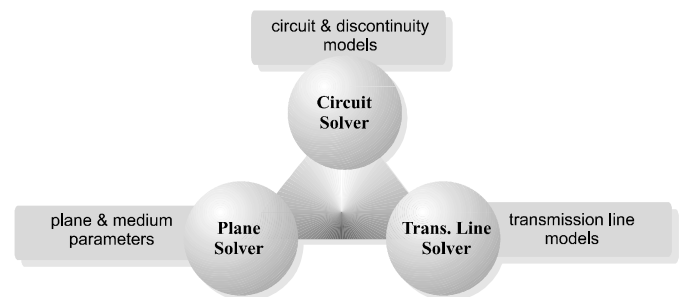


Figure 1. Components of the package simulator.

An efficient technique for the simulation of electromagnetic field propagation inside multi-layer packages has recently been developed [2]. It integrates circuit simulator, transmission line simulator and electromagnetic field solver using a special simultaneous linking scheme to provide a full-wave solution of the EM fields inside packages. Voltage variations at any points on power and ground planes are computed. Electromagnetic interactions such as package resonance, coupling between vias and coupling between traces, are taken into account in the simulation. The efficiency of this approach makes the evaluation of decoupling capacitors possible for real-world packaging structures.

### SIMULATION SCHEME

Our package simulator mainly consists of three solvers: the circuit, the transmission line, and the plane solvers as shown in Figure 1. The circuit solver computes all the lumped circuit components, such as resistors, capacitors, inductors, drivers, and receivers. The transmission line solver computes signal propagation along transmission lines such as strip and microstrip lines [3]. The plane solver computes transient

voltage and current distributions on metal planes [4]. The circuit, the transmission line and the plane solvers are run simultaneously, and properly linked together to take into account interactions between circuits, metal planes and signal vias/traces. An illustration of a multi-layer packaging structure and its computation components is shown in Figure 2.

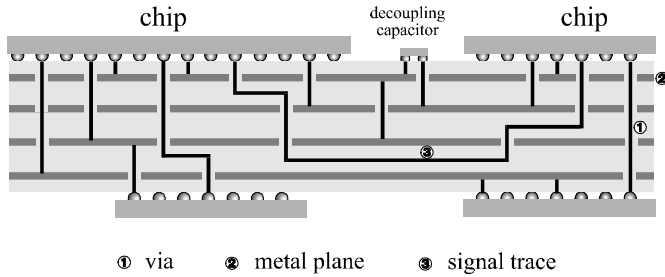


Figure 2(a). Multi-layer packaging structure.

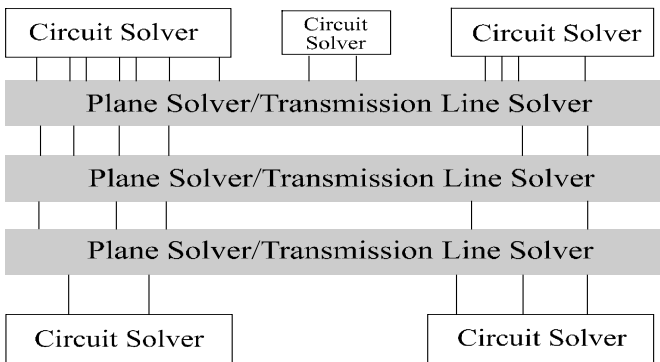


Figure 2(b). Computation components for the multi-layer power/ground plane structure.

The electromagnetic field simulation algorithms embedded in the plane solvers are derived from special geometric features of packaging structures. The electromagnetic field inside a typical multi-layered package is a three dimensional field in nature. However, it is not an arbitrary three dimensional field and can be decomposed into several modes each of which can be simulated with special techniques that are orders of magnitude faster than those for general 3-D fields. On the aspect of circuit analysis, we use the distributed

circuit solver that may include many individual circuit solvers instead of the traditional approach, which computes all the lumped circuit components associated with a package with one circuit solver (Figure 3). Circuit networks that are connected by package interconnects have their own circuit equations and are each solved by a designated circuit solver that is linked to the plane and the transmission line solvers. With the distributed circuit solver approach, each circuit solver deals with a relatively small size of circuit network, resulting in more efficient and stable circuit analysis.

The above technique has been developed as a general electrical simulation tool for packaging such as high-speed printed circuit board (PCB), single chip carrier, and multi-chip module (MCM). With given information like device switching parameters and package layout, the Delta-I noise distribution on any power/ground plane can be accurately and quickly simulated. By varying the value, the number and the placement of the decoupling capacitor, a few simulation runs can result in maximum noise suppression.

The strategy for the optimum placement of decoupling capacitors is simulating the whole structure, observing the electromagnetic field simulation results, and making adjustment on capacitor's value, location and number. With the tool, the spatial noise distributions on the power and ground planes can be visualized. The "hot-area", where voltage fluctuations are largest and decoupling capacitors are most wanted, can be clearly identified. The value of the decoupling capacitors can then be fine tuned until further increment of the decoupling capacitor value has virtually no effects on noise reduction. This procedure is applied repeatedly in the process of adding decoupling capacitors in a given package until the voltage fluctuations are below a pre-specified noise margin. An analogue to this process can be thought as you want to pin down a waving blanket, where the bouncing forces are from the switching drivers. And all you need to do is to determine where to put those pins - the decoupling capacitors, how many pins you need (or you are able) to put on, and how tight you want those pins to pin on the ground.

## EXAMPLES

### A. A Simple Example

Figure 5(a) shows a structure with one power and one ground plane, three source points and four sink points. The source points are connected with the switching current sources with pulse waveform shown in Figure 4. The sink points are assumed to be tied with ideal voltage supplies with zero source impedance. The physical parameters of the structure are the following: the power and ground planes are 100 mm by 100 mm in size, with a separation of 200  $\mu\text{m}$ ; the dielectric medium between the power and ground planes has a relative permittivity of 4; the via radius is 100  $\mu\text{m}$ .

After a simulation of the transient response of the above structure for a 20 ns time period, the peak voltage fluctuations at every point on the plane during this time period are shown as a surface plot in Figure 6(a). It can be clearly seen from

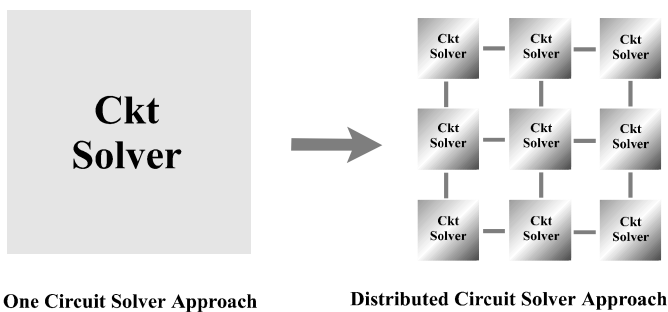


Figure 3. One circuit solver approach versus distributed circuit solvers approach.

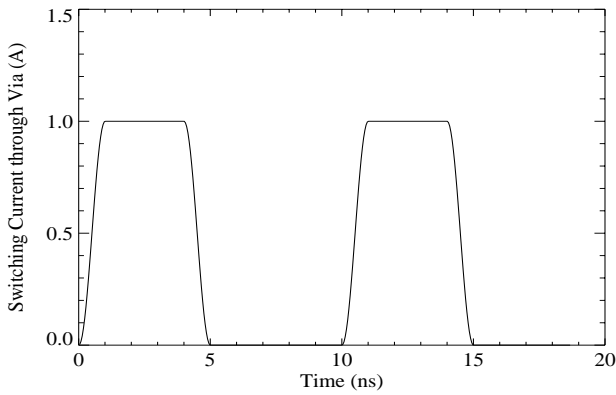


Figure 4. Waveform of the current source.

this peak noise distribution diagram that the source points are the forces driving the bouncing action and the ideal voltage supplies at four sink points holds up the reference voltage in limited areas. Figure 7 illustrates another way to measure the distribution of peak voltage fluctuations after statistical analysis are applied on the values of the peak noise voltages. The dotted line (marked as "no decap") in Figure 7 shows that the peak noise voltage on most area of the plane is between 1.0 V and 1.15 V and the maximum noise magnitude is about 1.2 V.

Then a decoupling capacitor was placed at the center of the plane (Figure 5(b)). The value of the capacitor was varied from 100 pF to 100 nF in several runs. The effectiveness of the capacitor with different values can be seen in Figure 7. In this case, there is no overall improvement when the value of the capacitor is greater than 10 nF. The noise on most of the area was redistributed around 0.5 V, when 10 nF decoupling capacitor was used, and the maximum noise was cut down to 0.6 V. The spatial distribution of the peak Delta-I noise with 10 nF decoupling capacitor is plotted in Figure 6(b), where the reduction of the Delta-I noise due to the capacitor can be clearly seen.

After 10 nF was selected as the proper value, more decoupling capacitors were placed. Figure 5(c) shows four peripheral locations around the source points are chosen for the extra

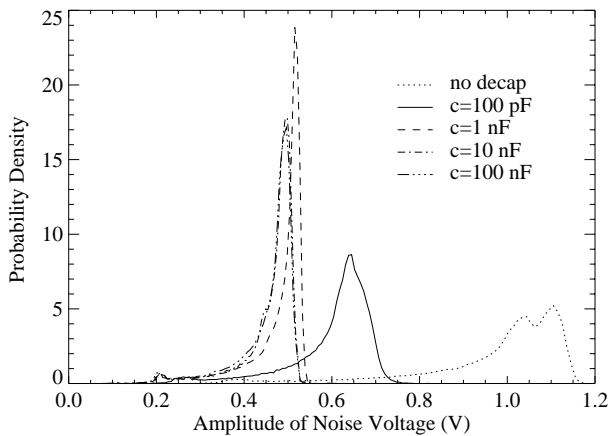


Figure 7. The statistical noise distribution for a capacitor with different values.

capacitors. As expected, the simulation results reveals that the Delta-I noise is further reduced to about 0.3 V, except those locations of switching sources (Figure 6(c)). The improvement on the peak noise distribution is shown in Figure 8.

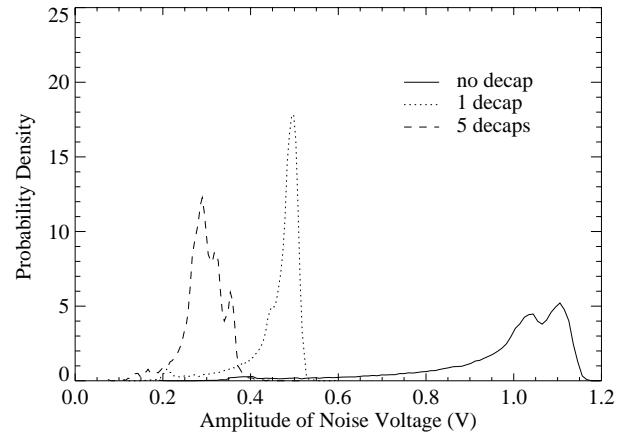


Figure 8. The statistical noise distribution from simulations with no decoupling capacitor, 1 capacitor and 5 capacitors.

### B. A Complex Example

In this example, a printed circuit board with one power plane and one ground plane is analyzed. The board is 120 mm by 80 mm. The separation between the power and the ground plane is 200  $\mu\text{m}$ . Vias are all 200  $\mu\text{m}$  in radius. All components are mounted on the top plane. Three IC chips all have multiple switching drivers. The big chip is in a 200-pin PGA package of 32 power pins, 136 output drivers, with 3 V voltage supply (Figure 9). Assume the worst situation when all the 136 12-mA drivers experience a low-to-high transition, the averaged switching current carried by a power pin is about 50 mA. The rise time of the low-to-high transition is assumed to be 600 ps. The two smaller chips are QFPs and each has 12 peripheral power pins, which also carry 50 mA switching current. Assume they switch simultaneously with the big chip, but with a slower rise time of 800 ps. All the signal lines have capacitor load of 2 pF. Four power pins near the right edge of the board are for an external connector, which supplies the ideal reference voltage.

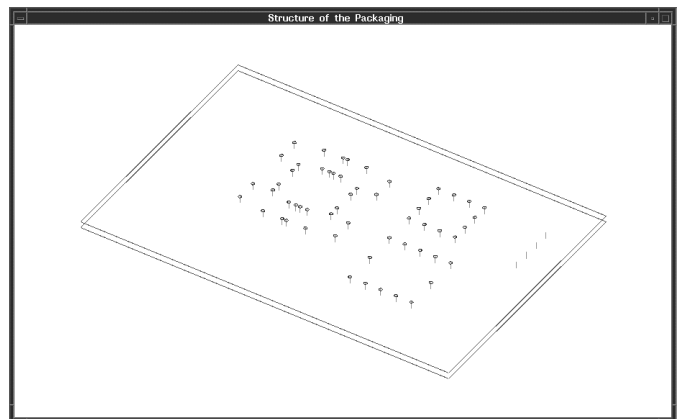


Figure 9. A printed circuit board with 3 IC chips.

The simulation with no decoupling capacitor on board result in voltage fluctuations spanning from 0 to 260 mV (solid line in Figure 10). After visualizing the surface plot of the peak noise from a 4 ns transient response, a hot-area was picked for placing the first testing decoupling capacitor. The testing value of the capacitor was set equal to 100 pF, 1nF, 10 nF, 100 nF, and 1  $\mu$ F. It was found that when the capacitor value was set beyond 1 nF, further increment had no improvement on Delta-I noise reduction. Therefore, 10 nF was chosen as a safe value for all the decoupling capacitors. Figure 10 is the statistical distribution of noise voltages associated with different capacitance values.

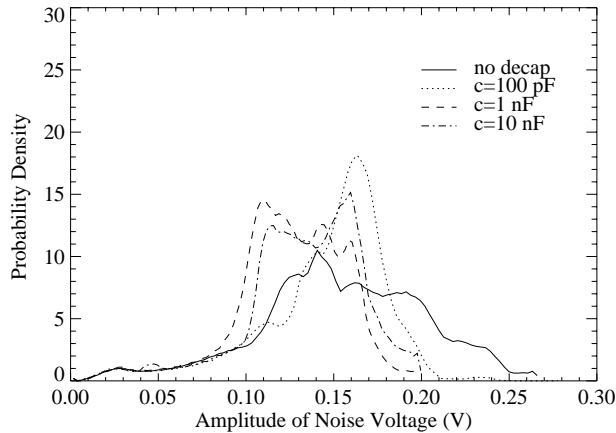


Figure 10. The statistical noise distribution for a decoupling capacitor with different values.

More decoupling capacitors were placed on the board after several simulations. These decoupling capacitors were placed near the switching sources to control the bouncing forces; or put at places where relative large voltage fluctuations were exhibited. It is assumed that all the capacitors are mounted on the top layer of the board, and no decoupling capacitors can be placed in the area occupied by the chips. After a total of 23 decoupling capacitors were placed on the board, the Delta-I noise was controlled below 100 mV on most area of the plane (Figure 11). The statistical noise distribution shown in Figure 12 illustrates the improvement of noise reduction with 10 and 23 decoupling capacitors.

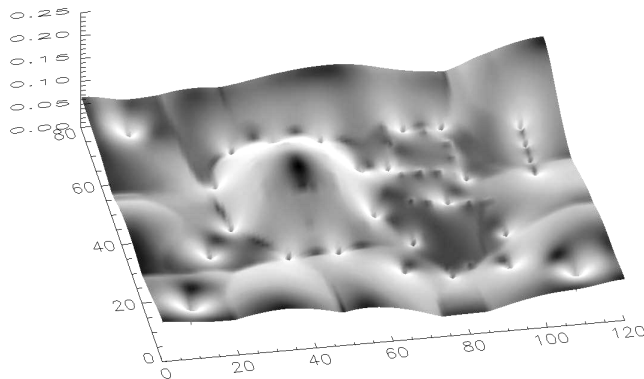


Figure 11. The spatial distribution of the peak noise voltage.

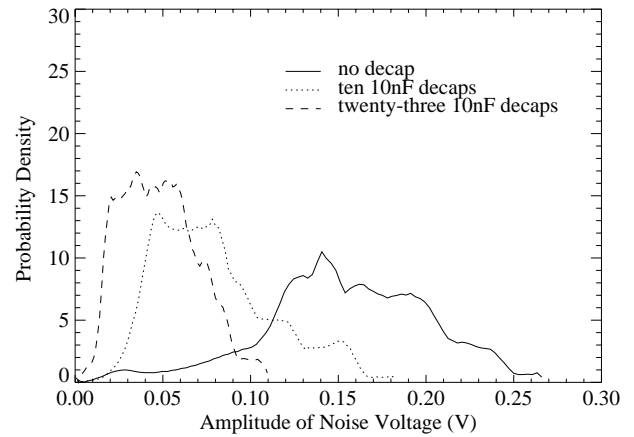


Figure 12. The statistical noise distribution from simulations with no decoupling capacitor, 10 capacitors and 23 capacitors.

## CONCLUSION

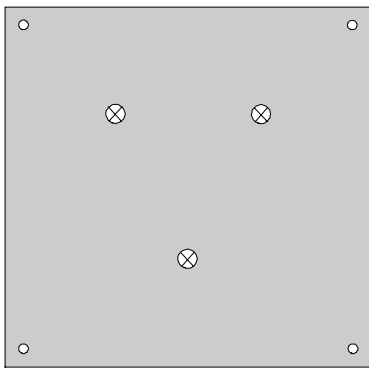
This paper demonstrates that, with simulation tools that are capable of performing efficient electromagnetic field analysis, effects of decoupling capacitors on packages and printed circuit boards can be evaluated. Such tools can guide design engineers determine the value, the number and the location of the capacitors to be placed. The statistical noise voltage distributions can be used to assess the effectiveness of decoupling capacitor placement.

## ACKNOWLEDGMENT

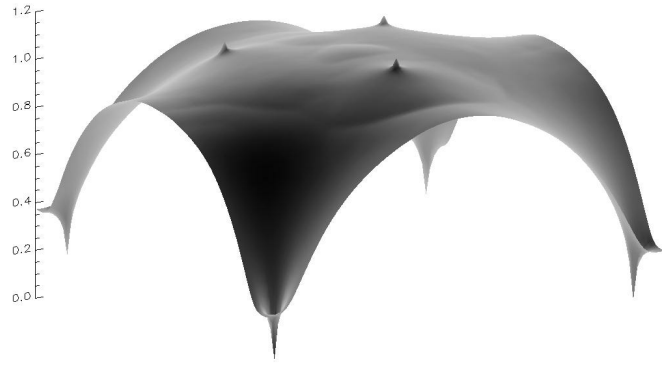
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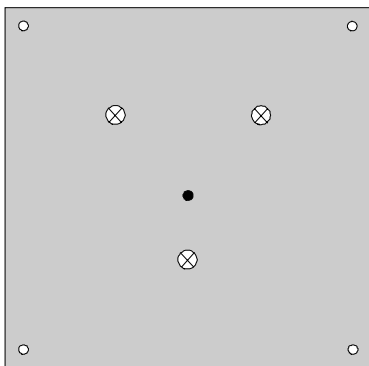
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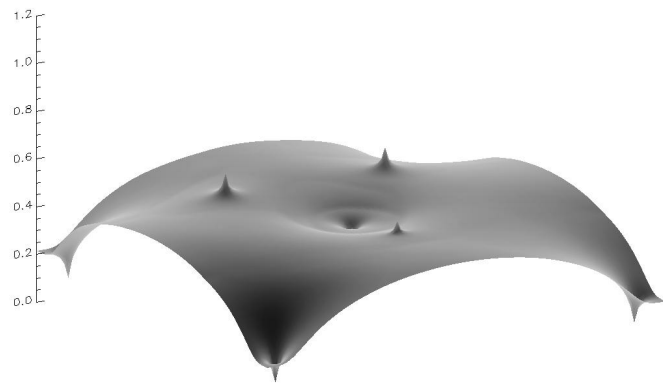
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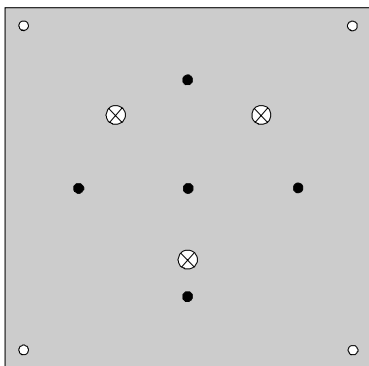
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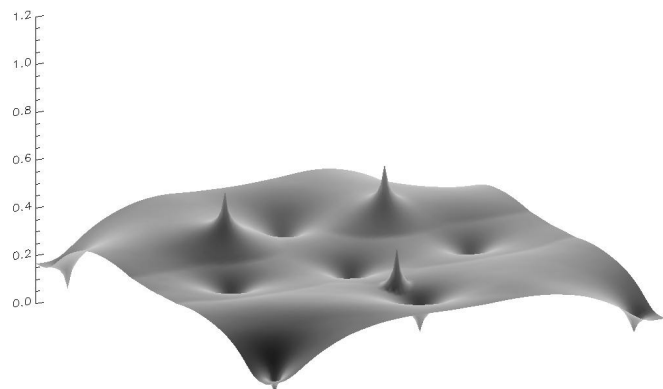
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b



c



c

- ⊗ source point
- sink point
- decoupling capacitor

Figure 5. Structures with no decoupling capacitor, 1 capacitor and 5 capacitors.

Figure 6. Spatial distribution of peak Delta-I noise.